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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,660	12/30/2003	Ashish Gupta	42P17993	9747

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,660	GUPTA ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/06;05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7,9-12,14-17,19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimelman et al. (US Publication Number 20040210804A1). As per claim 1, Kimelman et al. discloses a circuit to generate a training pattern; a debug circuit to generate debug information; and an information assembly unit to combine the training pattern with the debug information on page 1, paragraphs 0008-0009; on page 5, paragraph 0088.

3. As per claim 2, Kimelman et al. discloses further comprising a serializer unit to serialize the combined debug and training pattern information on page 1, paragraph 0009.

4. As per claim 3, Kimelman et al. discloses further comprising an output circuit to drive the combined debug and training pattern information onto an interconnect on page 1, paragraphs 0009-0010.

5. As per claim 4, Kimelman et al. discloses the output circuit to drive the combined debug and training pattern information onto a high-speed

asynchronous interconnect on page 1, paragraphs 0009-0010; on page 5, paragraph 0088.

6. As per claim 5, Kimelman et al. discloses the training pattern to include parity information on page 5, paragraph 0088.

7. As per claim 6, Kimelman et al. discloses the serializer unit to reduce the debug and training pattern information down to 10 wires on page 5, paragraph 0082.

8. As per claim 7, Kimelman et al. discloses the output circuit to output 10 bits at a time onto the interconnect on page 5, paragraphs 0082,0088.

9. As per claim 9, Kimelman et al. discloses an input circuit to receive combined debug and training pattern information over an interconnect; and a de-serialization unit to receive the debug and training information from the input circuit; and a data extraction unit coupled to the de-serialization unit to separate the debug information from the training pattern information on page 1, paragraphs 0008-0009; on page 5, paragraph 0088; on page 7, paragraph 0123.

10. As per claim 10, Kimelman et al. discloses further comprising a buffer to receive the separated debug information from the data extraction unit on page 7, paragraph 0123.

11. As per claim 11, Kimelman et al. discloses further comprising a memory controller coupled to the buffer, the memory controller to transmit the debug information over a memory bus on page 7, paragraph 0121; on page 4, paragraph 0071.

12. As per claim 12, Kimelman et al. discloses the input circuit to receive 10 bits at a time from the interconnect on page 5, paragraphs 0082,0088.

13. As per claim 14, Kimelman et al. discloses a transmitting device including a circuit to generate a training pattern, a debug circuit to generate debug information, an information assembly unit to combine the training pattern with the debug information, and a serializer unit to serialize the combined debug and training pattern information; and a receiving device coupled to the transmitting device via an interconnect, the receiving device including an input circuit to receive the combined debug and training pattern information over an interconnect, and a de-serialization unit to receive the debug and training information from the input circuit, and a data extraction unit coupled to the de-serialization unit to separate the debug information from the training pattern information in Figure 1,5; on page 1, paragraphs 0008-0009; on page 5, paragraph 0088; on page 7, paragraph 0123.

14. As per claim 15, Kimelman et al. discloses the transmitting device further including an output circuit to drive the combined debug and training pattern information onto the interconnect on page 1, paragraphs 0008-0010.

15. As per claim 16, Kimelman et al. discloses wherein the interconnect is a high-speed asynchronous interconnect on page 5, paragraph 0088.

16. As per claim 17, Kimelman et al. discloses the output circuit to output 10 bits at a time onto the interconnect on page 5, paragraphs 0082,0088.

17. As per claim 19, Kimelman et al. discloses combining debug information with a training pattern; serializing the combined information; and outputting the

serialized debug and training information onto an interconnect on page 1, paragraphs 0008-0009; on page 5, paragraph 0088.

18. As per claim 20, Kimelman et al. discloses wherein combining debug information with a training pattern includes combining debug information with a training pattern that includes parity information on page 5, paragraph 0088.

19. As per claim 21, Kimelman et al. discloses wherein serializing the combined information includes reducing the combined information down to 10 wires on page 5, paragraph 0082.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 8,13,18,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimelman et al. in view of Wikipedia (packet). As per claims 8,13,18,22, Kimelman et al. discloses the debug and training pattern information organized into 80 bit packets, where 72 bits are debug information and 8 bits are training pattern information.

Wikipedia discloses this limitation on page 1, under Packet mechanism, "Different communications protocols...byte level."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the debug and training pattern information organized into 80 bit packets, where 72 bits are debug information and 8 bits are training pattern information. A person of ordinary skill in the art would have been motivated to have the debug and training pattern information organized into 80 bit packets, where 72 bits are debug information and 8 bits are training pattern information because packets can be organized by way of the communications protocols used within the systems they are being transferred through.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Examiner
Art Unit 2113